LM833-N Dual Audio Operational Amplifier

Check for Samples: LM833-N

FEATURES

- **Wide Dynamic Range: >140dB**
- **Low Input Noise Voltage: 4.5nV/√Hz**
- **High Slew Rate: 7 V/μs (typ); 5V/μs (Min)**
- **High Gain Bandwidth: 15MHz (typ); 10MHz (Min)**
- **Wide Power Bandwidth: 120KHz**
- **Low Distortion: 0.002%**
- **Low Offset Voltage: 0.3mV**
- **Large Phase Margin: 60°**
- **Available in 8 Pin VSSOP Package**

DESCRIPTION

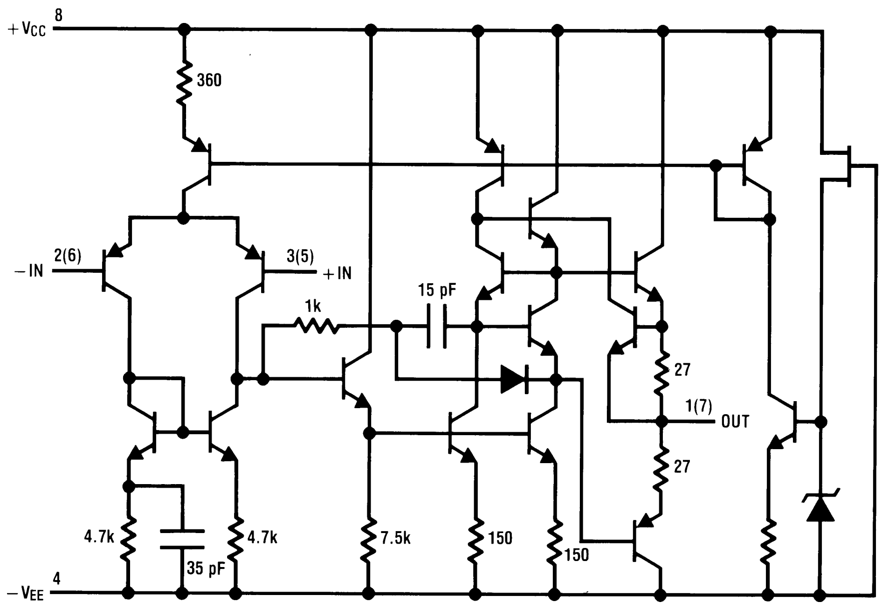
The LM833-N is a dual general purpose operational amplifier designed with particular emphasis on performance in audio systems.

This dual amplifier IC utilizes new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833-N is internally compensated for all closed loop gains and is therefore optimized for all preamp and high level stages in PCM and HiFi systems.

The LM833-N is pin-for-pin compatible with industry standard dual operational amplifiers.

Schematic Diagram

(1/2 LM833-N)



Connection Diagram

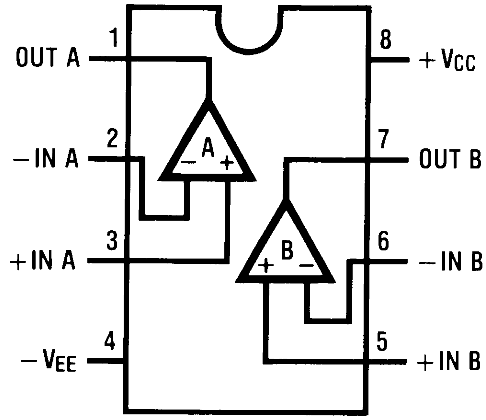


Figure 1. See Package Number D0008A, P0008E or DGK0008A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[(1)(2)]

Supply Voltage V_{CC}–V_{EE}			36V
Differential Input Voltage[(3)] V_I			±30V
Input Voltage Range[(3)] V_{IC}			±15V
Power Dissipation[(4)] P_D			500 mW
Operating Temperature Range T_{OPR}			−40 ~ 85°C
Storage Temperature Range T_{STG}			−60 ~ 150°C
Soldering Information	PDIP Package	Soldering (10 seconds)	260°C
	Small Outline Package (SOIC and VSSOP)	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
ESD tolerance [(5)]			1600V

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) If supply voltage is less than ±15V, it is equal to supply voltage.
(4) This is the permissible value at $T_A \leq 85°C$.
(5) Human body model, 1.5 kΩ in series with 100 pF.

DC ELECTRICAL CHARACTERISTICS[(1)(2)]

(T_A = 25°C, V_S = ±15V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 10Ω		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Voltage Gain	R_L = 2 kΩ, V_O = ±10V	90	110		dB
V_{OM}	Output Voltage Swing	R_L = 10 kΩ	±12	±13.5		V
		R_L = 2 kΩ	±12	±13.4		V
V_{CM}	Input Common-Mode Range		±12	±14.0		V
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±12V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 15 ~ 5V, −15 ~ −5V	80	100		dB
I_Q	Supply Current	V_O = 0V, Both Amps		5	8	mA

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_S = ±15V, R_L = 2 kΩ)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	R_L = 2 kΩ	5	7		V/μs
GBW	Gain Bandwidth Product	f = 100 kHz	10	15		MHz
V_{NI}	Equivalent Input Noise Voltage (LM833AM, LM833AMX)	RIAA, R_S = 2.2 kΩ[(1)]			1.4	μV

(1) RIAA Noise Voltage Measurement Circuit

DESIGN ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_S = ±15V)

The following parameters are not tested or ensured.

Symbol	Parameter	Conditions	Typ	Units
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage		2	μV/°C
THD	Distortion	R_L = 2 kΩ, f = 20~20 kHz V_{OUT} = 3 Vrms, A_V = 1	0.002	%
e_n	Input Referred Noise Voltage	R_S = 100Ω, f = 1 kHz	4.5	nV / $\sqrt{Hz}$
i_n	Input Referred Noise Current	f = 1 kHz	0.7	pA / $\sqrt{Hz}$
PBW	Power Bandwidth	V_O = 27 V_{pp}, R_L = 2 kΩ, THD ≤ 1%	120	kHz
f_U	Unity Gain Frequency	Open Loop	9	MHz
φ_M	Phase Margin	Open Loop	60	deg
	Input Referred Cross Talk	f = 20~20 kHz	−120	dB

TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Power Dissipation vs Ambient Temperature

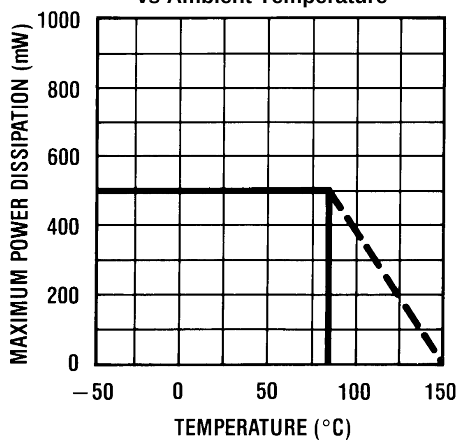


Figure 2.

Input Bias Current vs Ambient Temperature

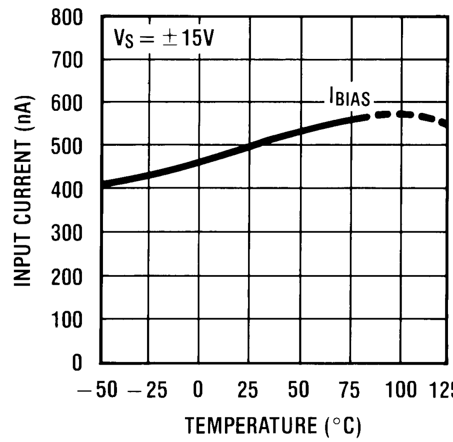


Figure 3.

Input Bias Current vs Supply Voltage

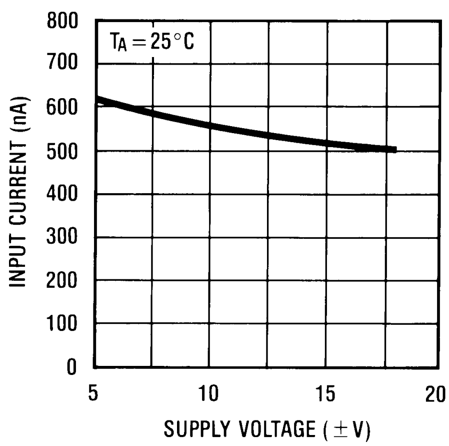


Figure 4.

Supply Current vs Supply Voltage

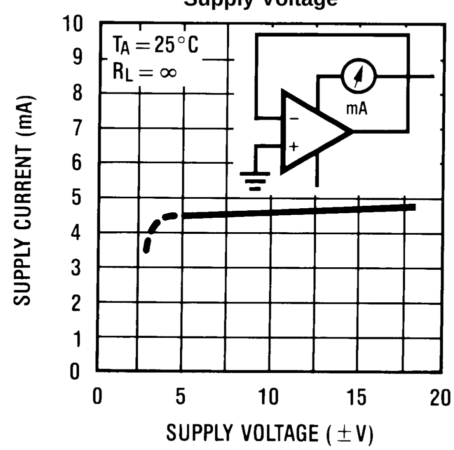


Figure 5.

DC Voltage Gain vs Ambient Temperature

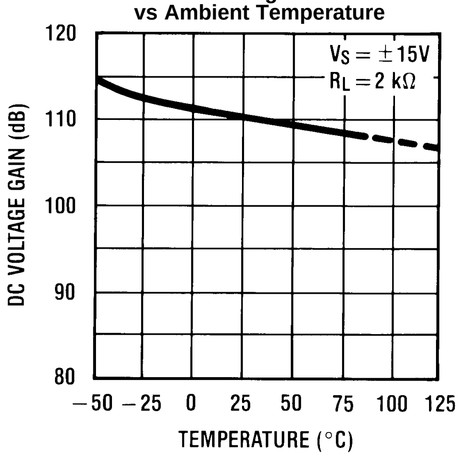


Figure 6.

DC Voltage Gain vs Supply Voltage

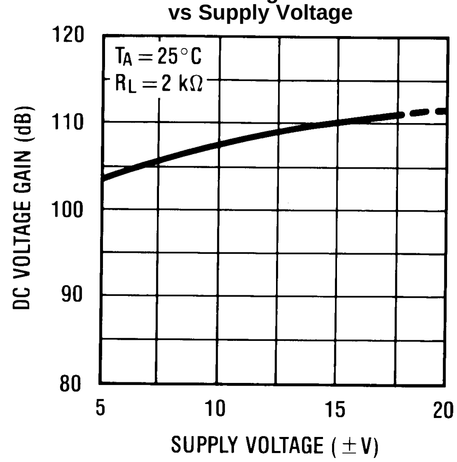


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Voltage Gain & Phase vs Frequency

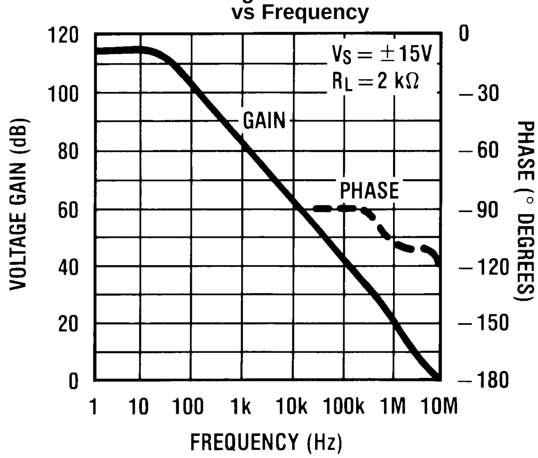


Figure 8.

Gain Bandwidth Product vs Ambient Temperature

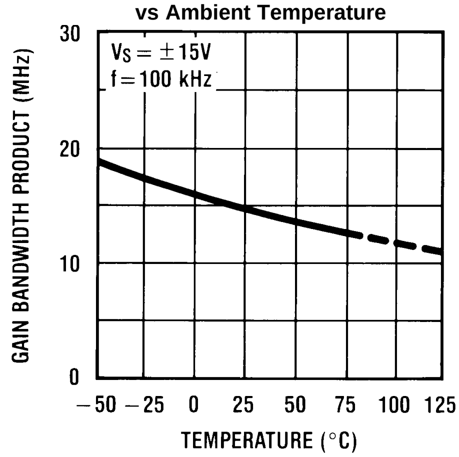


Figure 9.

Gain Bandwidth vs Supply Voltage

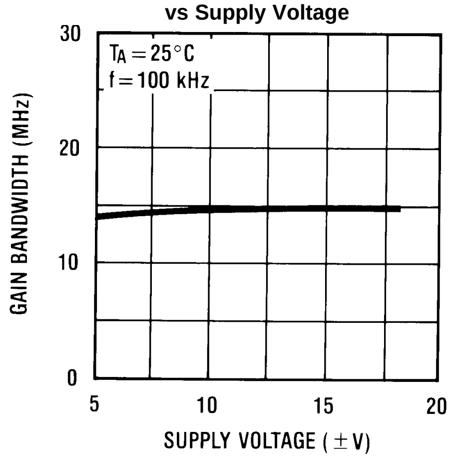


Figure 10.

Slew Rate vs Ambient Temperature

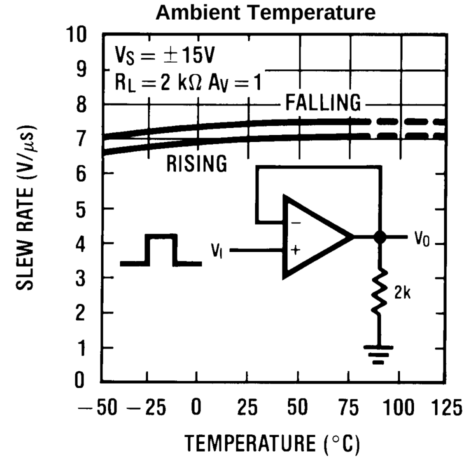


Figure 11.

Slew Rate vs Supply Voltage

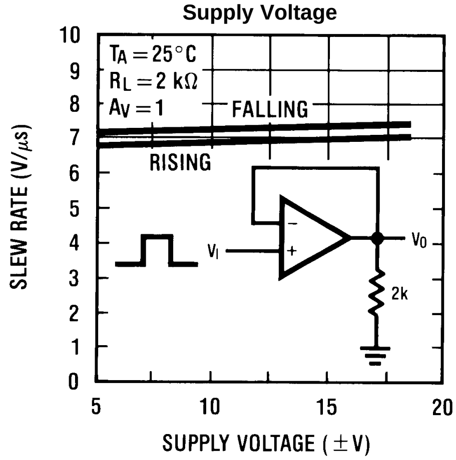


Figure 12.

Power Bandwidth

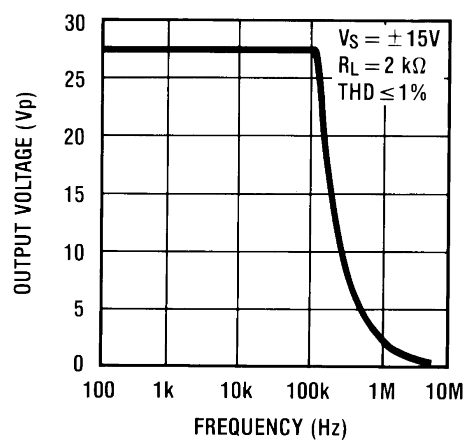


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

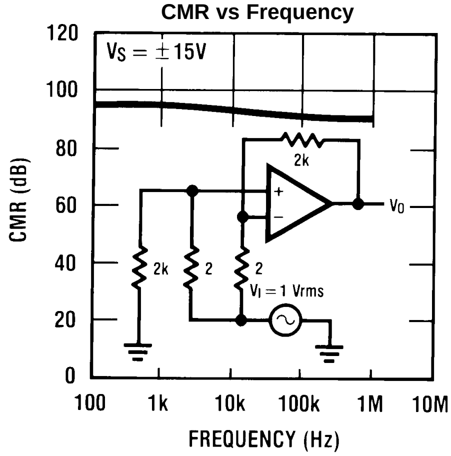


Figure 14.

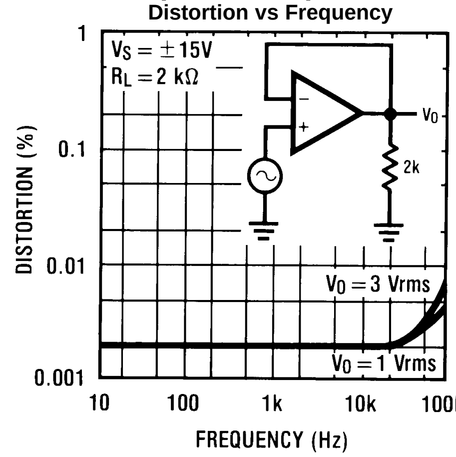


Figure 15.

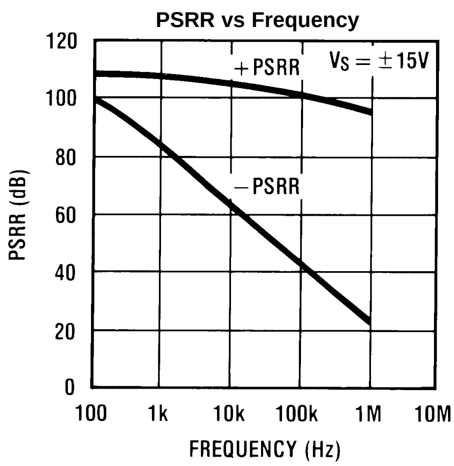


Figure 16.

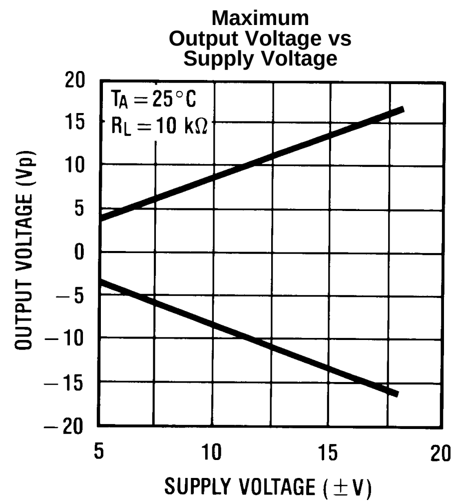


Figure 17.

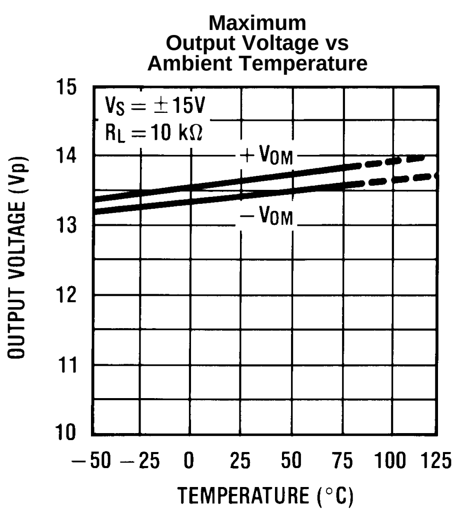


Figure 18.

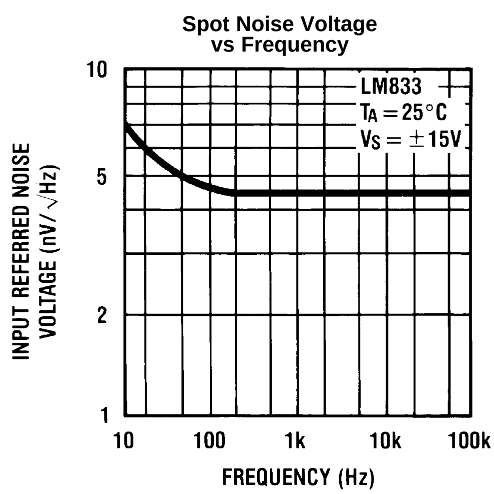


Figure 19.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Spot Noise Current vs Frequency

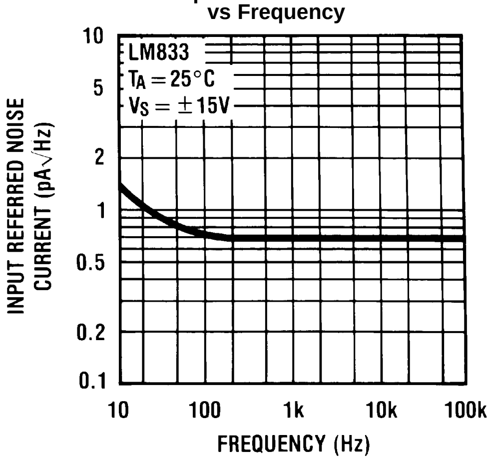


Figure 20.

Input Referred Noise Voltage vs Source Resistance

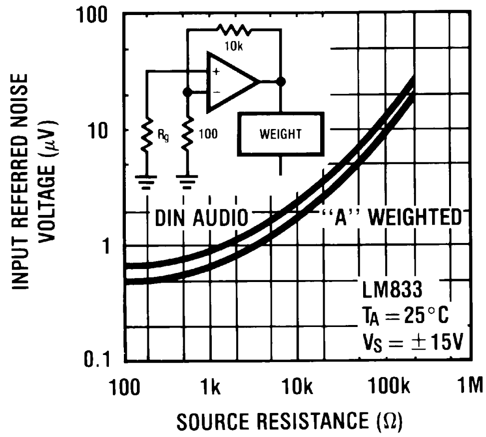


Figure 21.

Noninverting Amp

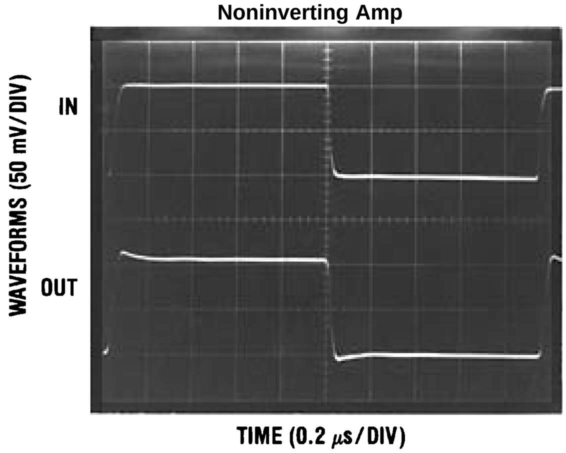


Figure 22.

Noninverting Amp

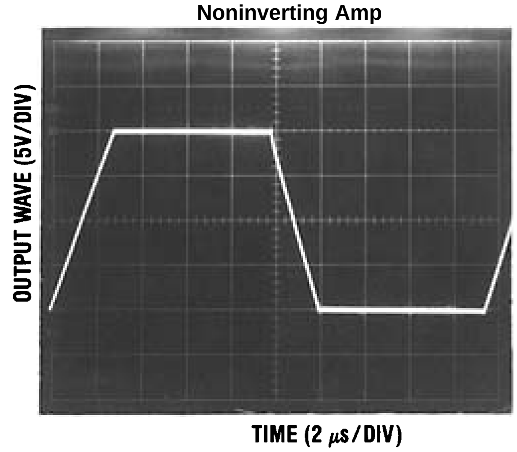


Figure 23.

Inverting Amp

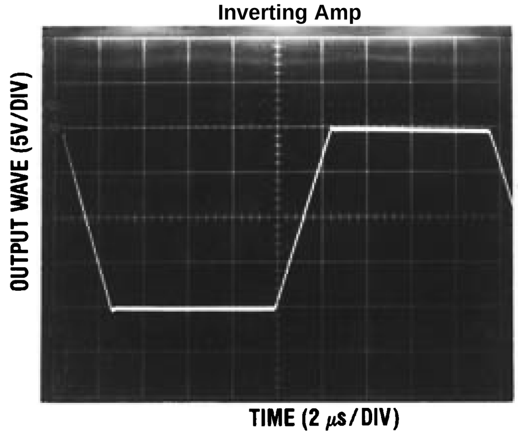


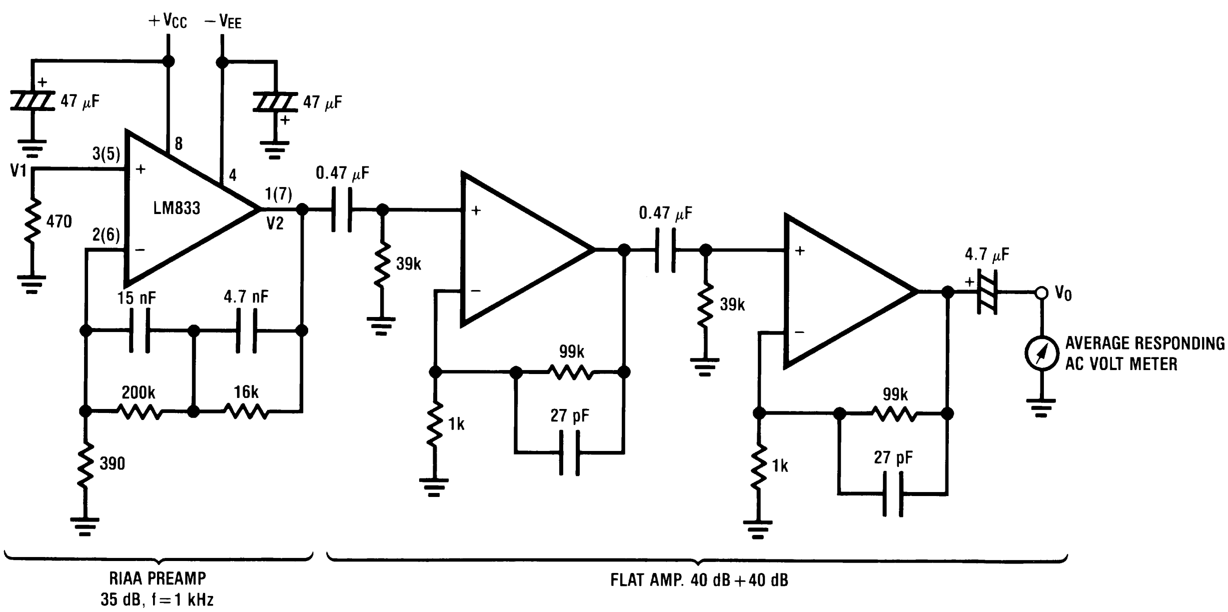
Figure 24.

APPLICATION HINTS

The LM833-N is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 50 pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 50 pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

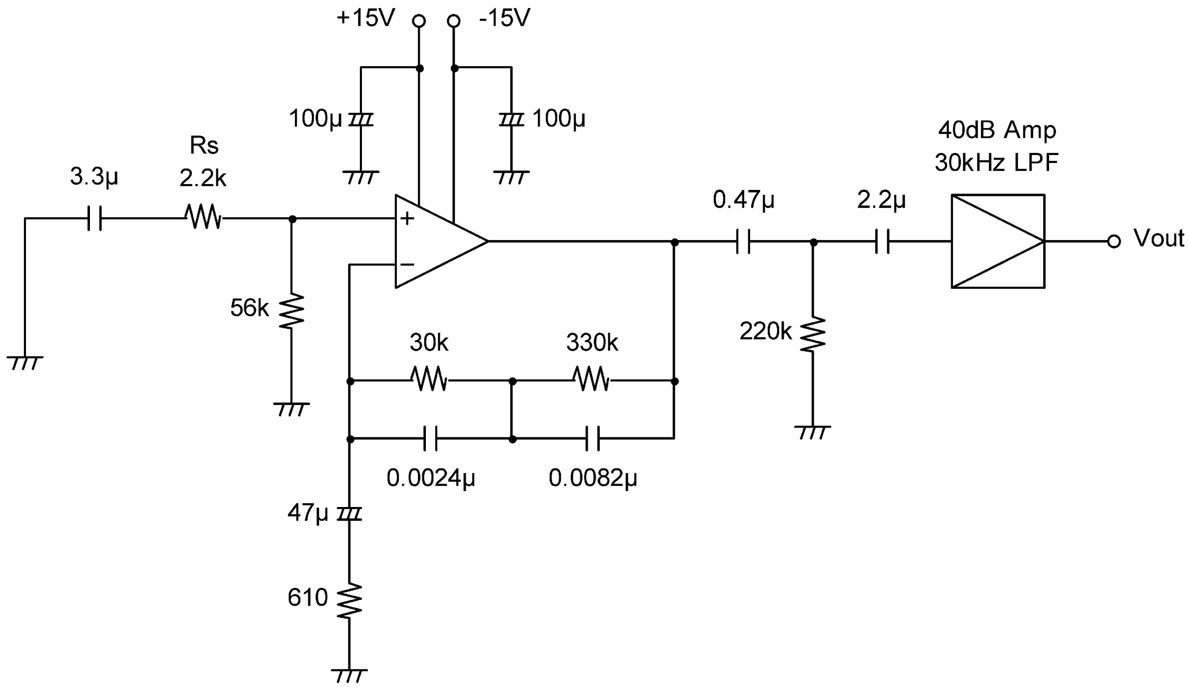
Noise Measurement Circuit



Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.

Figure 25. Total Gain: 115 dB @f = 1 kHz
Input Referred Noise Voltage: e_n = V0/560,000 (V)

RIAA Noise Voltage Measurement Circuit



RIAA Preamp Voltage Gain, RIAA Deviation vs Frequency

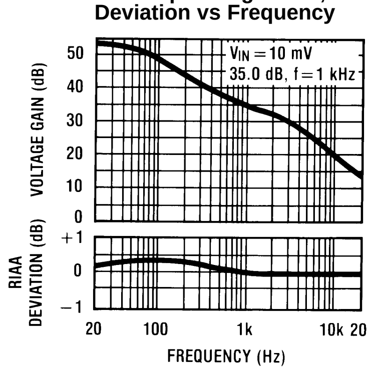


Figure 26.

Flat Amp Voltage Gain vs Frequency

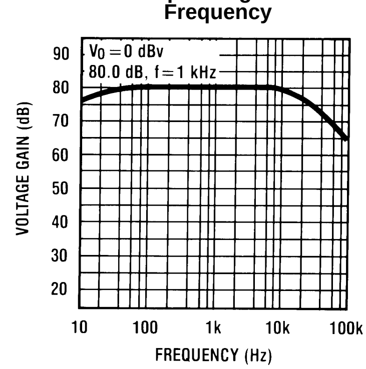
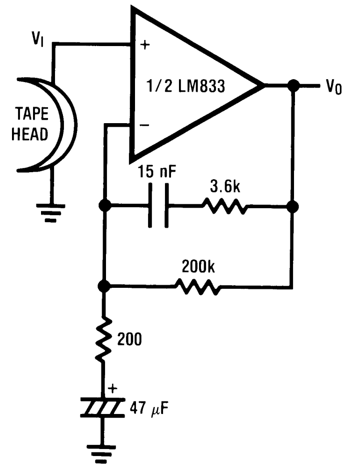


Figure 27.

Typical Applications



$A_V = 34.5$
F = 1 kHz
$E_n = 0.38\ \mu V$
A Weighted

Figure 28. NAB Preamp

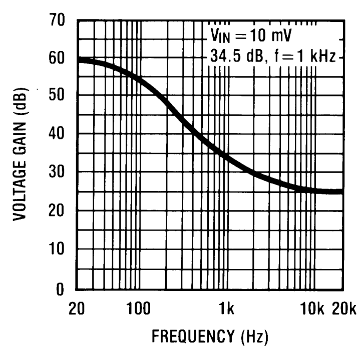
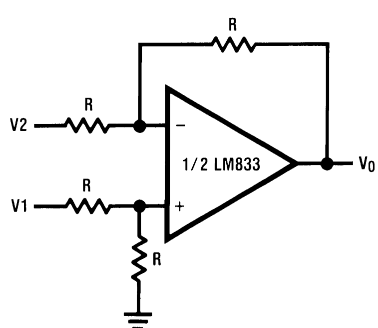
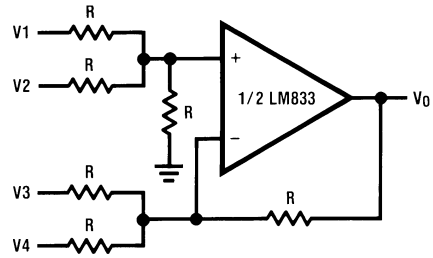


Figure 29. NAB Preamp Voltage Gain vs Frequency



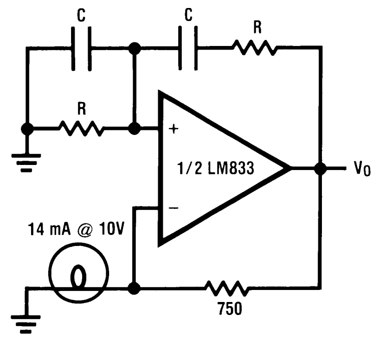
$V_O = V1–V2$

Figure 30. Balanced to Single Ended Converter



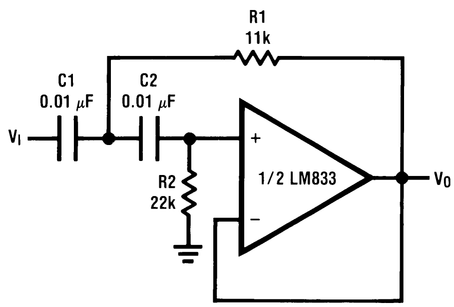
V_O = V1 + V2 − V3 − V4

Figure 31. Adder/Subtracter



$$f_o = \frac{1}{2\pi RC}$$

Figure 32. Sine Wave Oscillator



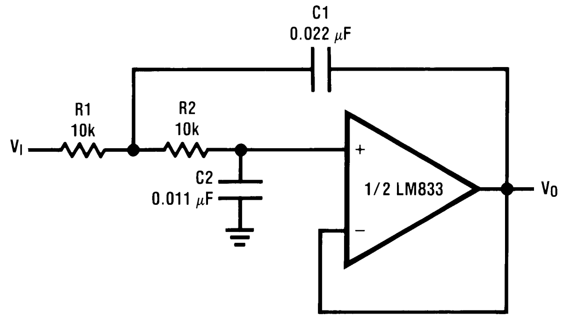
if C1 = C2 = C

$$R1 = \frac{\sqrt{2}}{2\omega_o C}$$

R2 = 2•R1

Illustration is f_0 = 1 kHz

Figure 33. Second Order High Pass Filter (Butterworth)



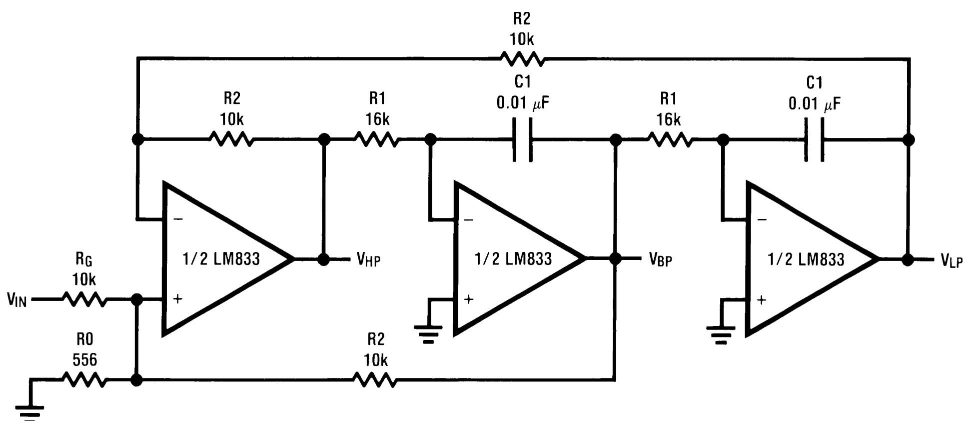
$$\text{if } R1 = R2 = R$$

$$C1 = \frac{\sqrt{2}}{\omega_o R}$$

$$C2 = \frac{C1}{2}$$

Illustration is f_0 = 1 kHz

Figure 34. Second Order Low Pass Filter (Butterworth)



$$f_0 = \frac{1}{2\pi C1R1},\ Q = \frac{1}{2}\left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right),\ A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

Illustration is f_0 = 1 kHz, Q = 10, A_{BP} = 1

Figure 35. State Variable Filter

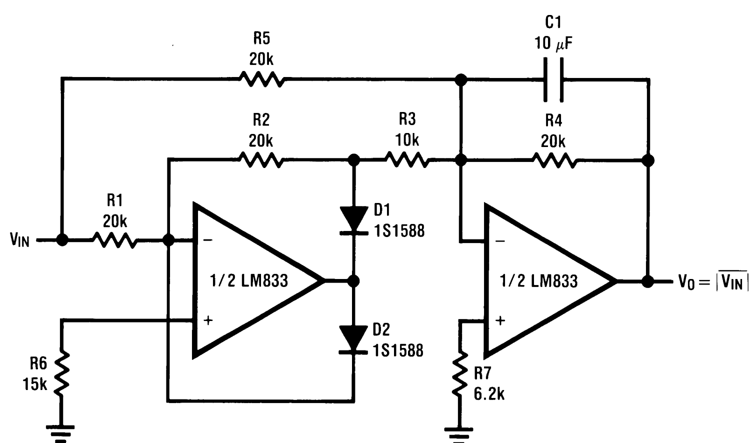


Figure 36. AC/DC Converter

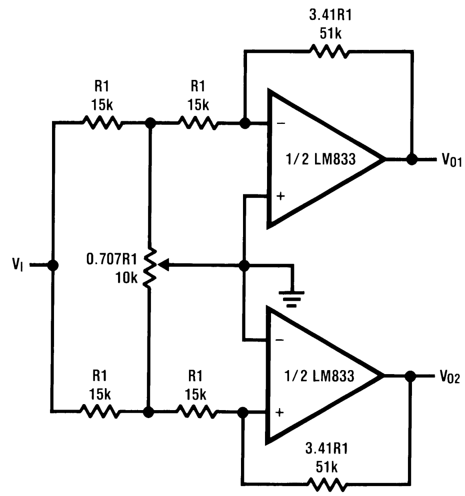


Figure 37. 2 Channel Panning Circuit (Pan Pot)

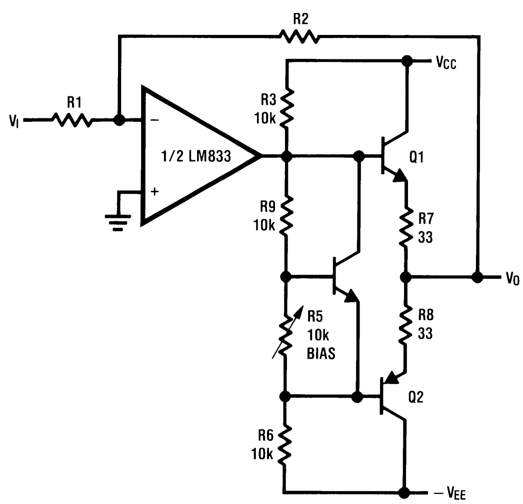
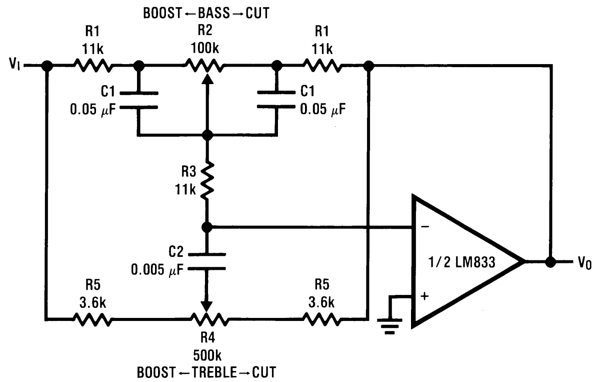


Figure 38. Line Driver



$$f_L = \frac{1}{2\pi R2C1}, \; f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C2}, \; f_{HB} = \frac{1}{2\pi (R1 + R5 + 2R3)C2}$$

Illustration is:
f_L = 32 Hz, f_{LB} = 320 Hz
f_H =11 kHz, f_{HB} = 1.1 kHz

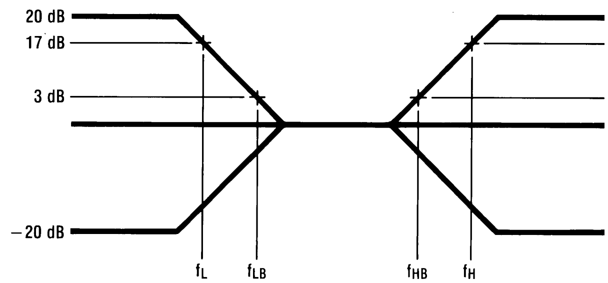
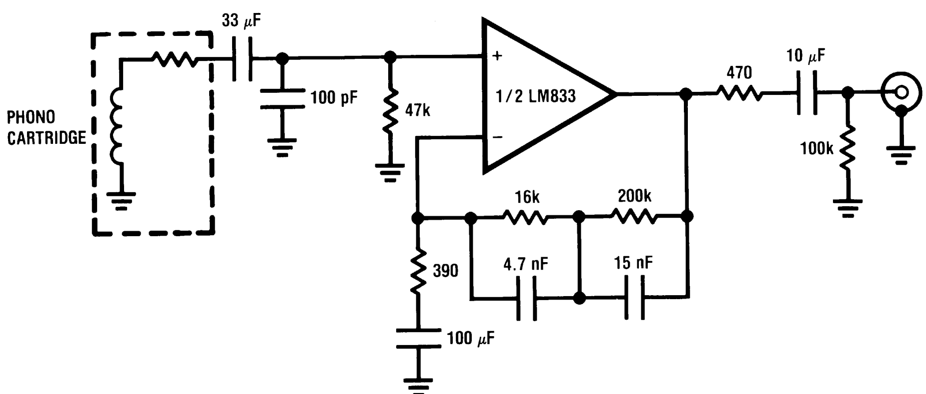
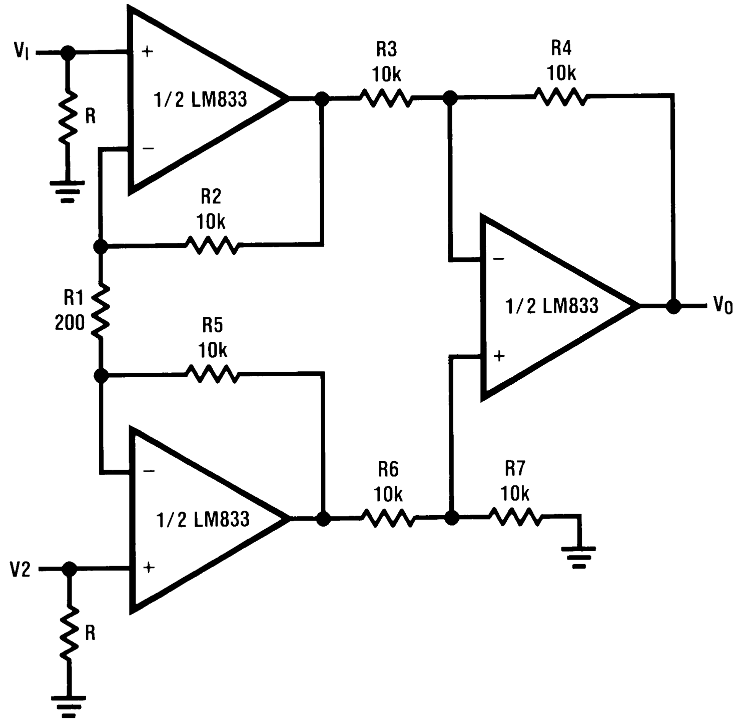


Figure 39. Tone Control



A_v = 35 dB
E_n = 0.33 μV
S/N = 90 dB
f = 1 kHz
A Weighted
A Weighted, V_{IN} = 10 mV
@f = 1 kHz

Figure 40. RIAA Preamp



If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

Illustration is:
V0 = 101(V2 − V1)

Figure 41. Balanced Input Mic Amp

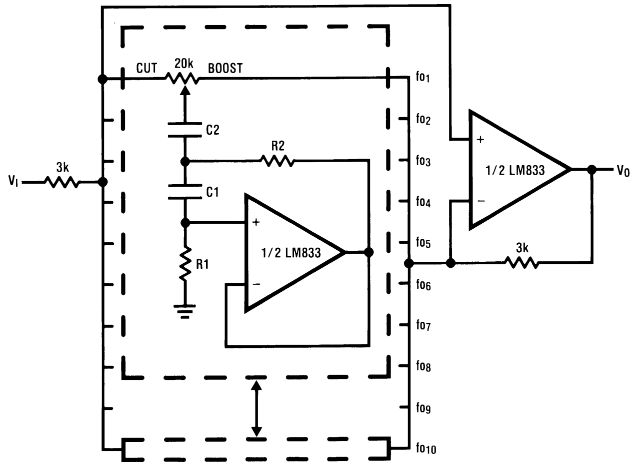


Figure 42. 10 Band Graphic Equalizer

fo (Hz)	C_1	C_2	R_1	R_2
32	0.12μF	4.7μF	75kΩ	500Ω
64	0.056μF	3.3μF	68kΩ	510Ω
125	0.033μF	1.5μF	62kΩ	510Ω
250	0.015μF	0.82μF	68kΩ	470Ω
500	8200pF	0.39μF	62kΩ	470Ω
1k	3900pF	0.22μF	68kΩ	470Ω
2k	2000pF	0.1μF	68kΩ	470Ω
4k	1100pF	0.056μF	62kΩ	470Ω
8k	510pF	0.022μF	68kΩ	510Ω
16k	330pF	0.012μF	51kΩ	510Ω

Note: At volume of change = ±12 dB Q = 1.

LM833-N MDC MWC DUAL AUDIO OPERATIONAL AMPLIFIER

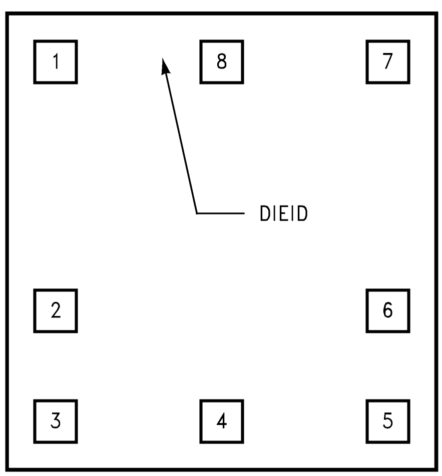


Figure 43. Die Layout (A - Step)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM833M	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM833 M	Samples
LM833M/NOPB	LIFEBUY	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM833 M	
LM833MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	Z83	Samples
LM833MMX/NOPB	LIFEBUY	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	Z83	
LM833MX	LIFEBUY	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LM833 M	
LM833MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM833 M	Samples
LM833N/NOPB	LIFEBUY	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LM 833N	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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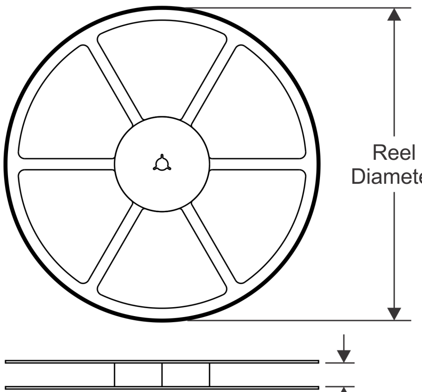
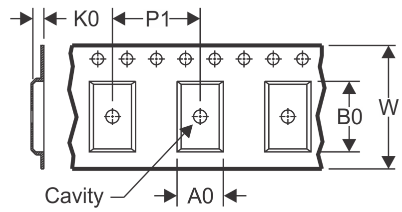
TAPE AND REEL INFORMATION

REEL DIMENSIONS

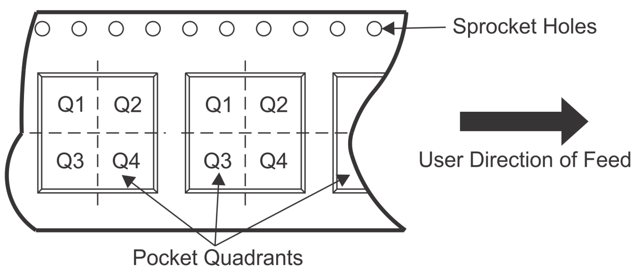


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

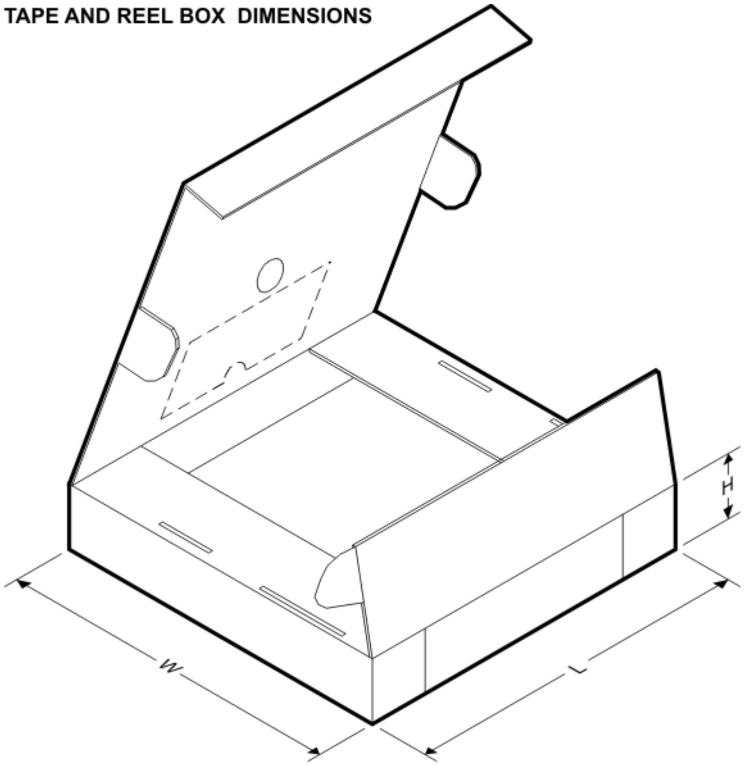
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM833MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM833MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM833MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM833MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

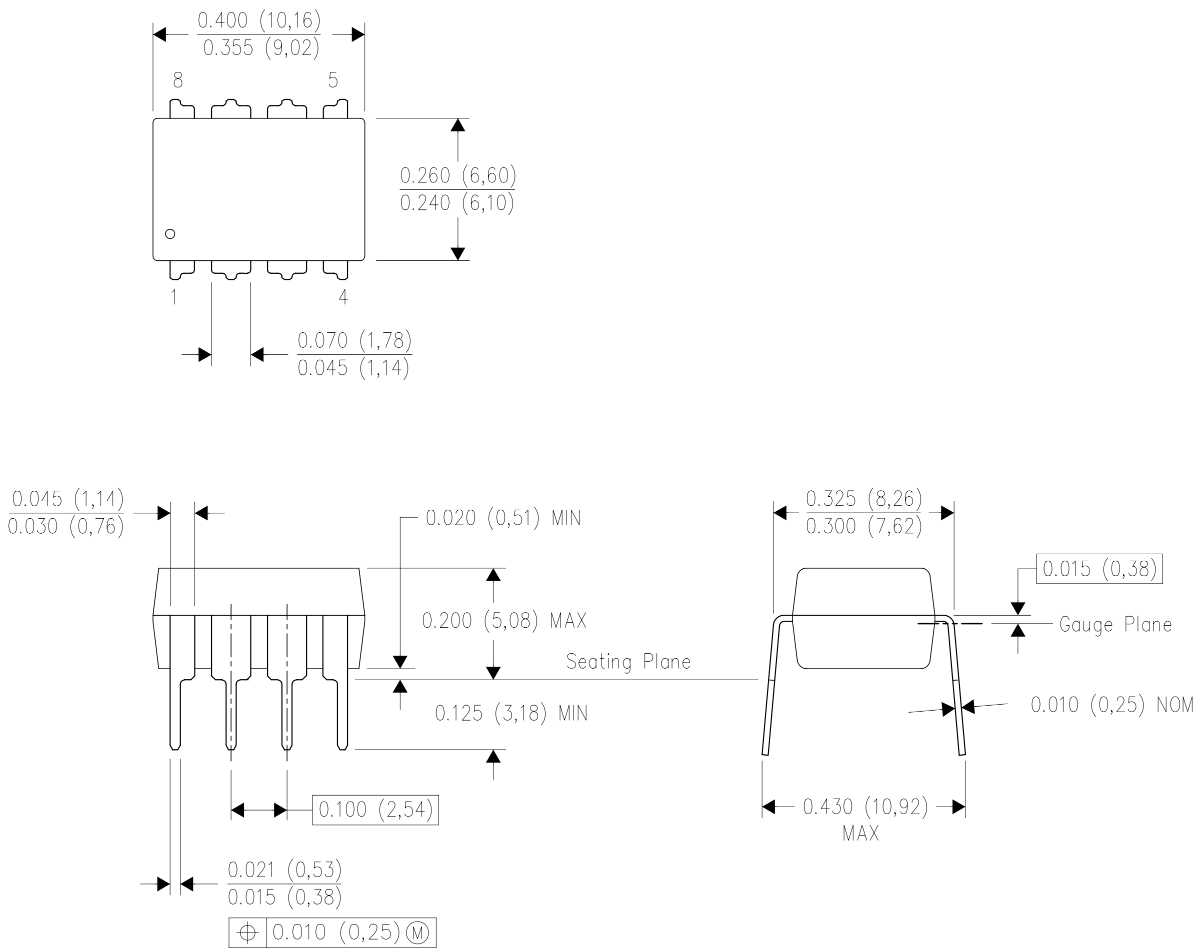
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM833MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM833MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM833MX	SOIC	D	8	2500	367.0	367.0	35.0
LM833MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

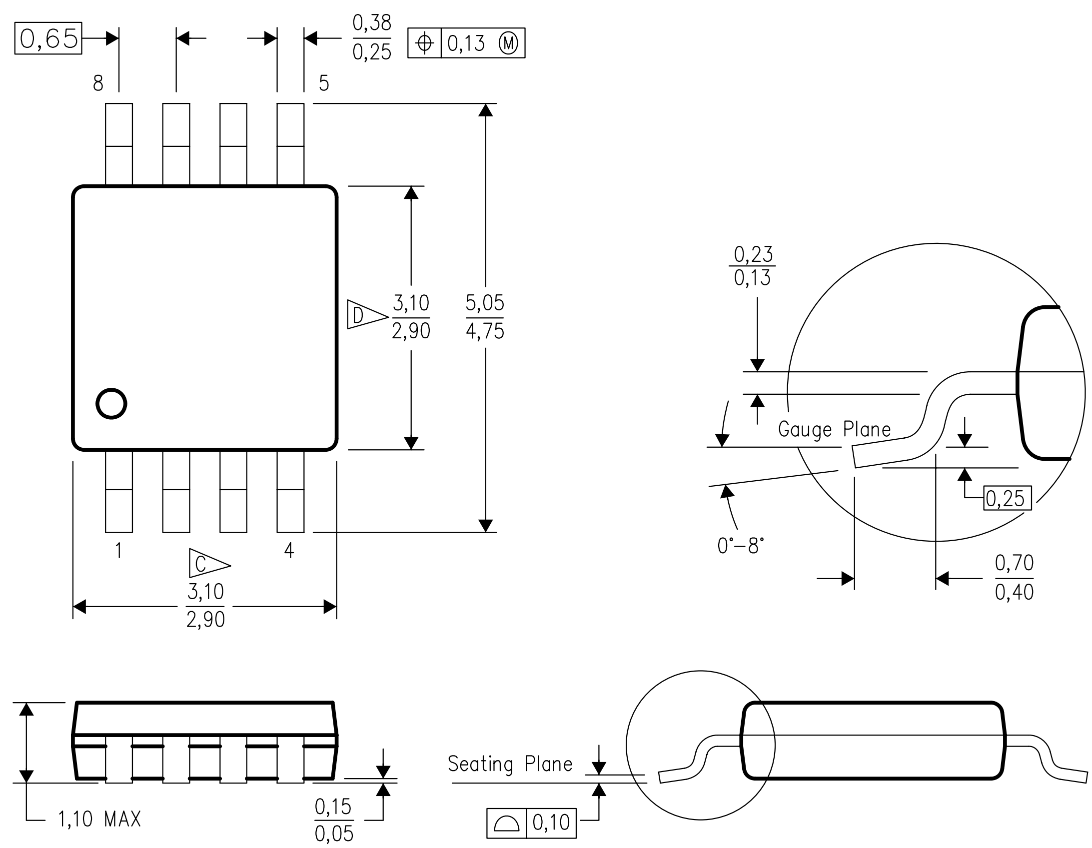
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

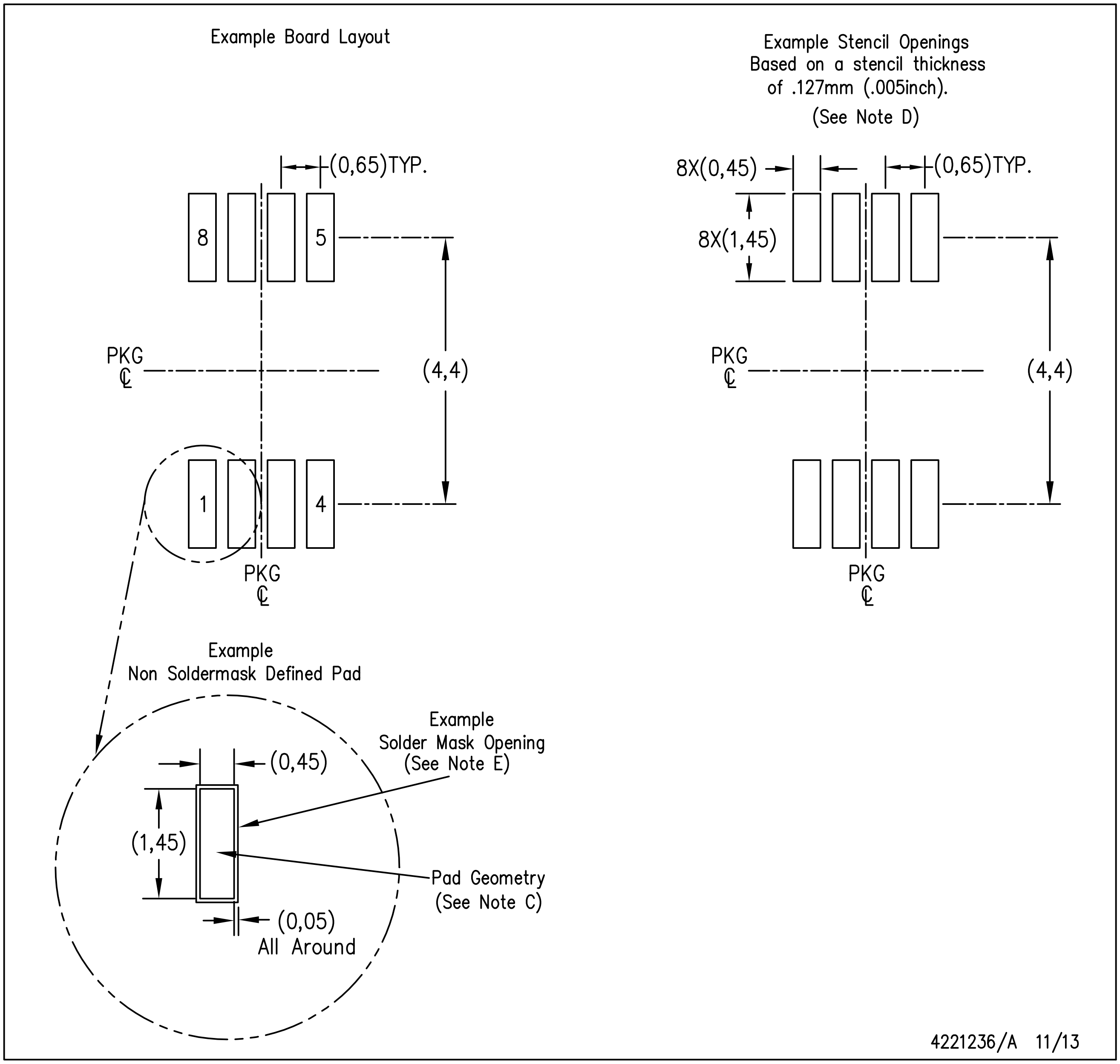
DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

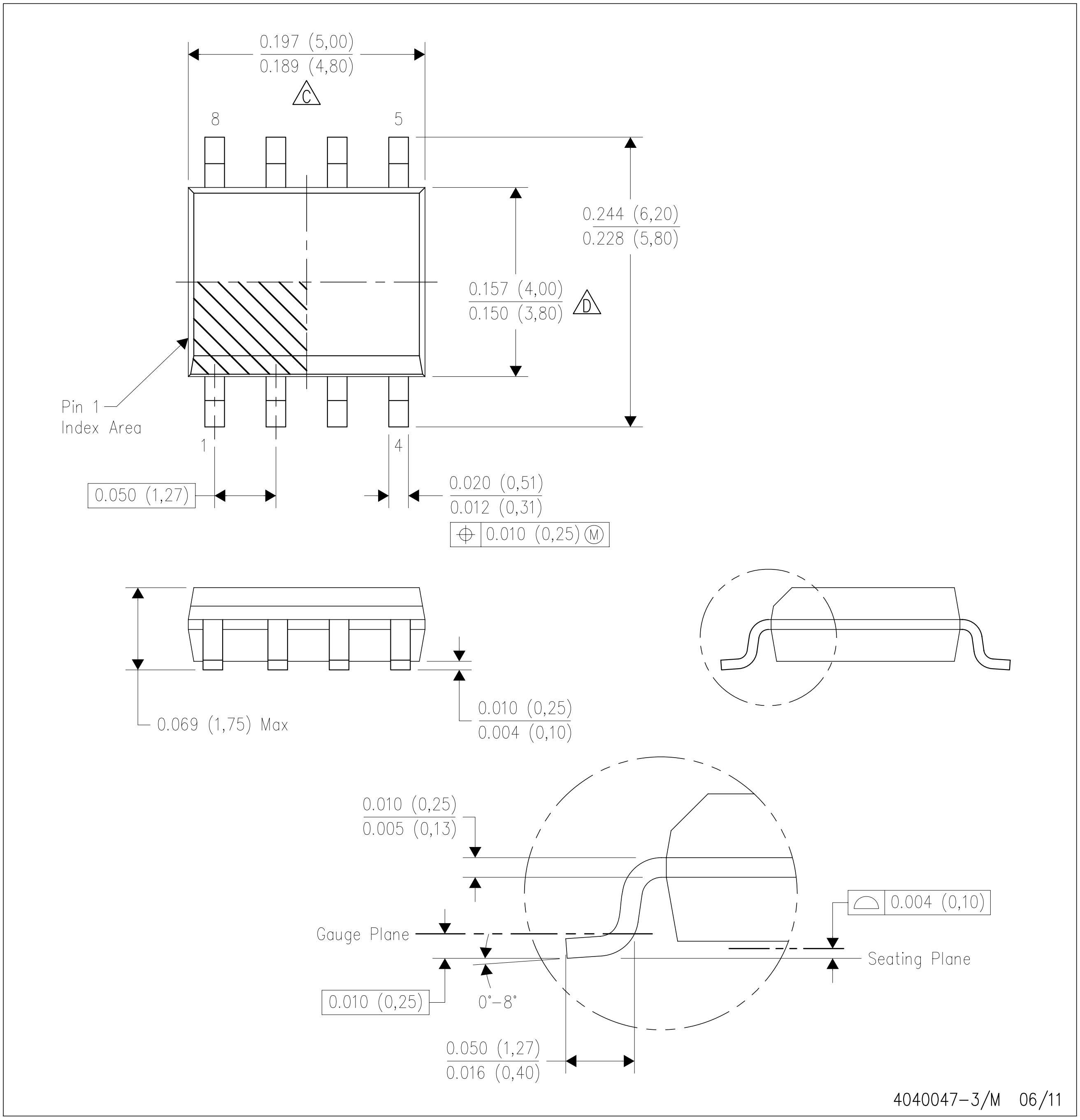
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

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